Fig. 1

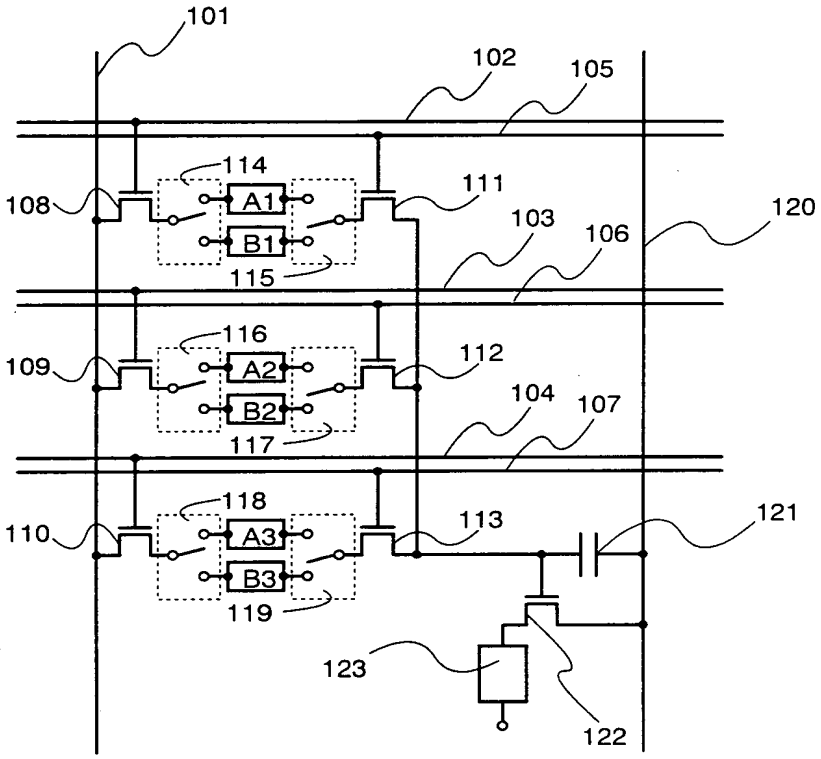

101
102
105
114
A1
B1
108
111
120
103
106
115
116
A2
B2
109
112
104
107
117
118
A3
B3
110
113
121
119
123
122

Fig. 2

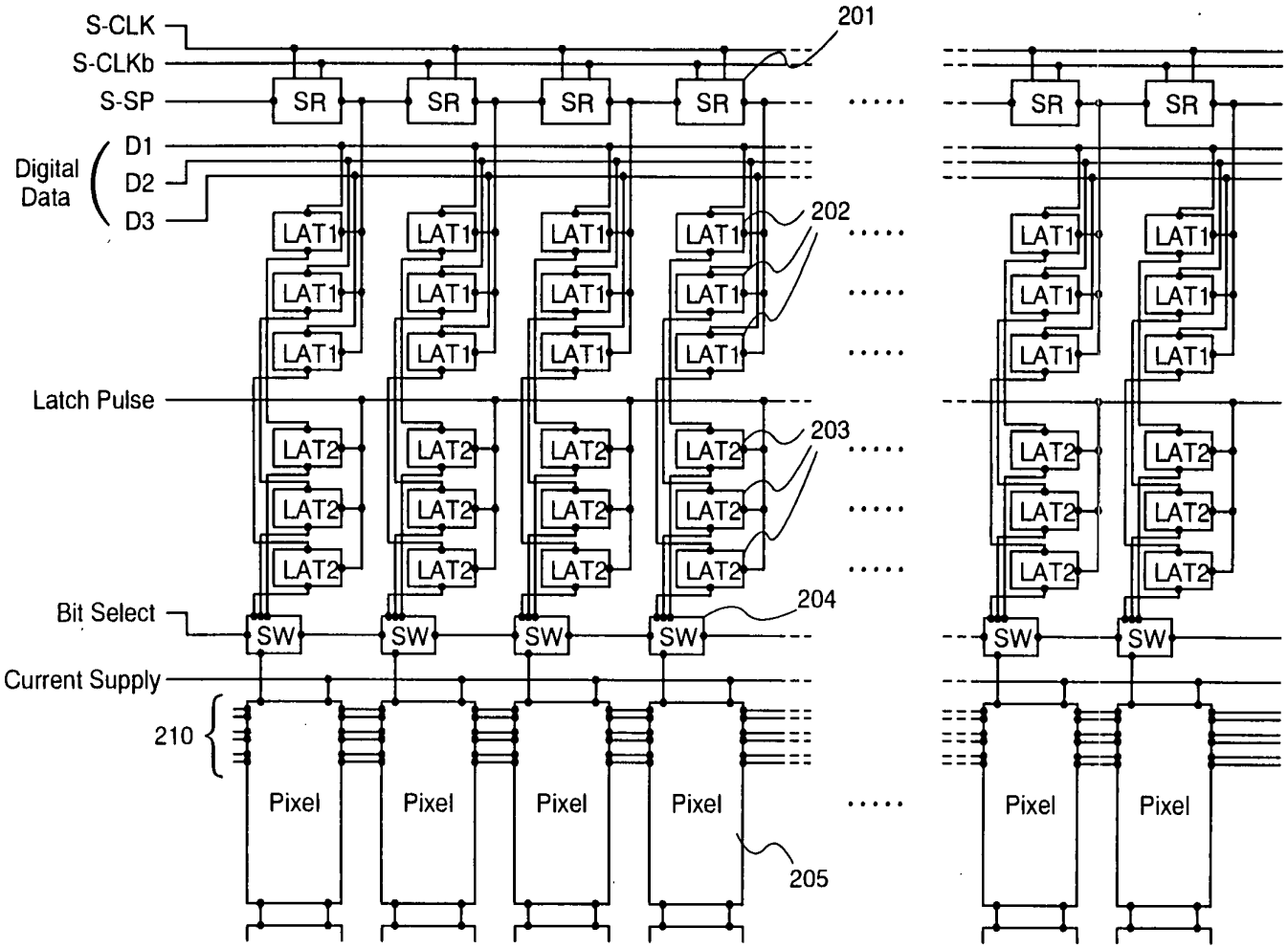

S-CLK
S-CLKb
S-SP
Digital Data
D1
D2
D3
Latch Pulse
Bit Select
Current Supply
210
SR
LAT1
LAT2
SW
Pixel
201
202
203
204
205

Fig. 3A

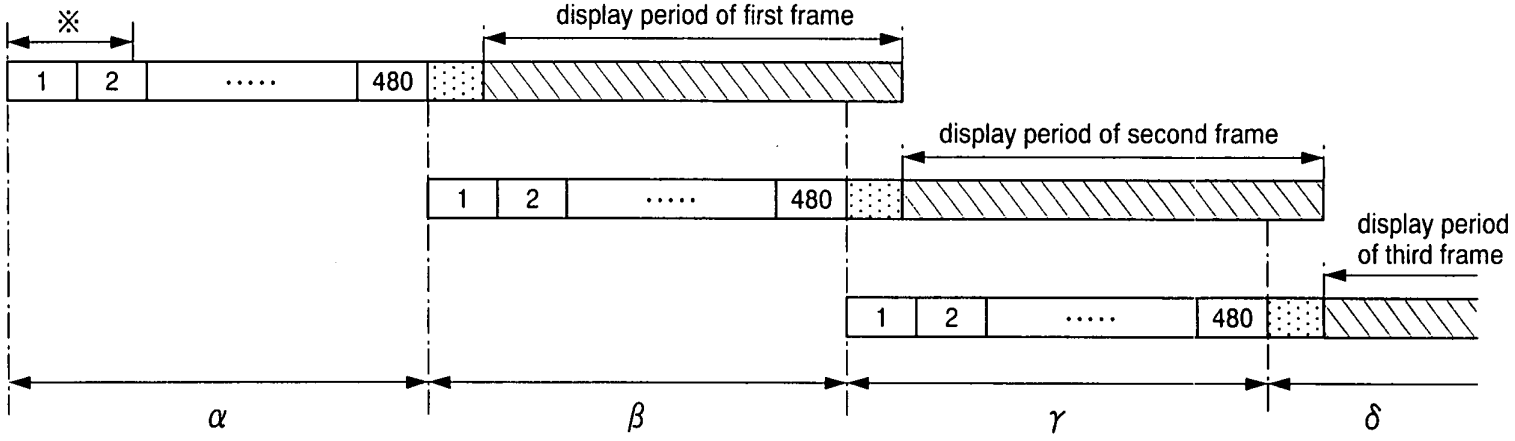


Fig. 3B

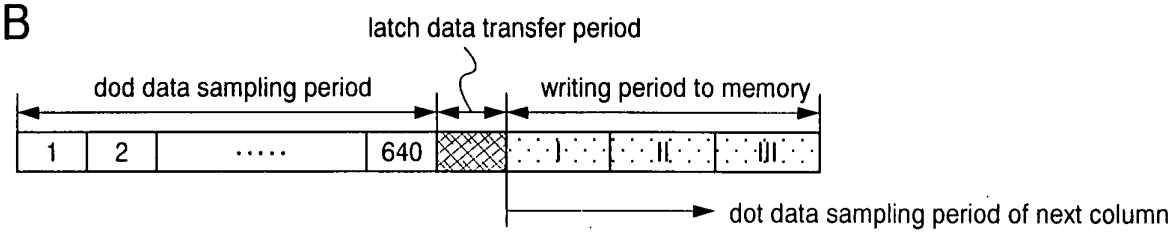


Fig. 3C

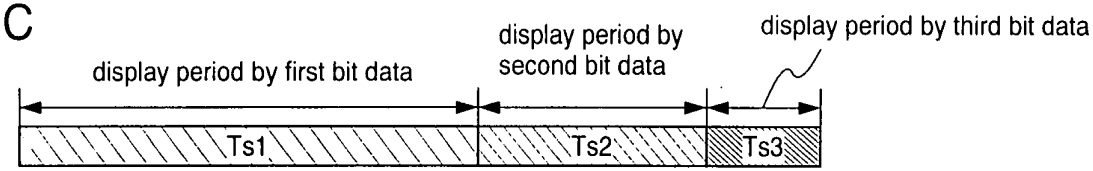


Fig. 4A

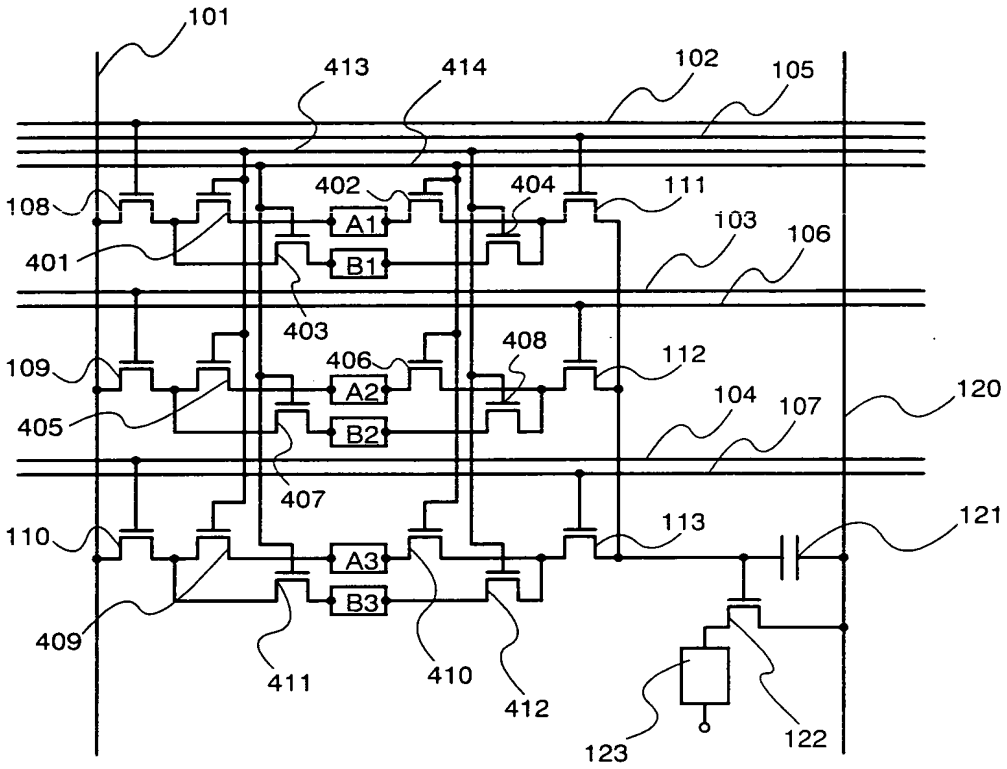

101
413
414
102
105
108
402
404
111
A1
401
B1
103
106
403
109
406
408
112
A2
405
B2
104
107
120
407
110
113
121
A3
B3
409
411
410
412
123
122

Fig. 4B

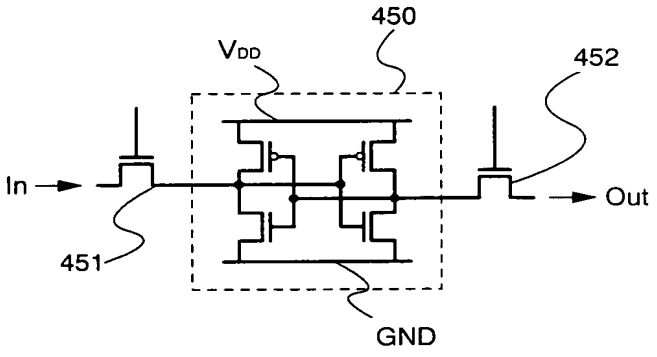

450
VDD
452
In
Out
451
GND

Fig. 5

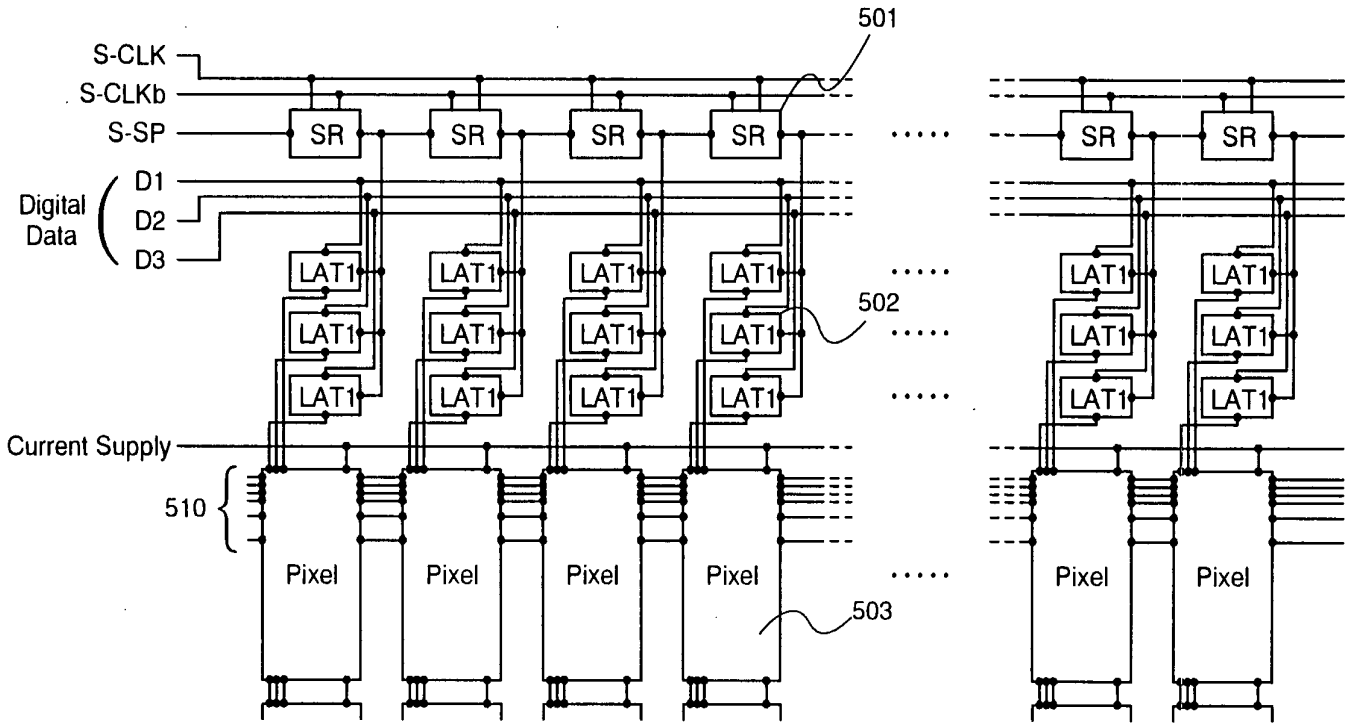

501
S-CLK
S-CLKb
S-SP
SR
Digital Data
D1
D2
D3
LAT1
502
Current Supply
510
Pixel
503

Fig. 6

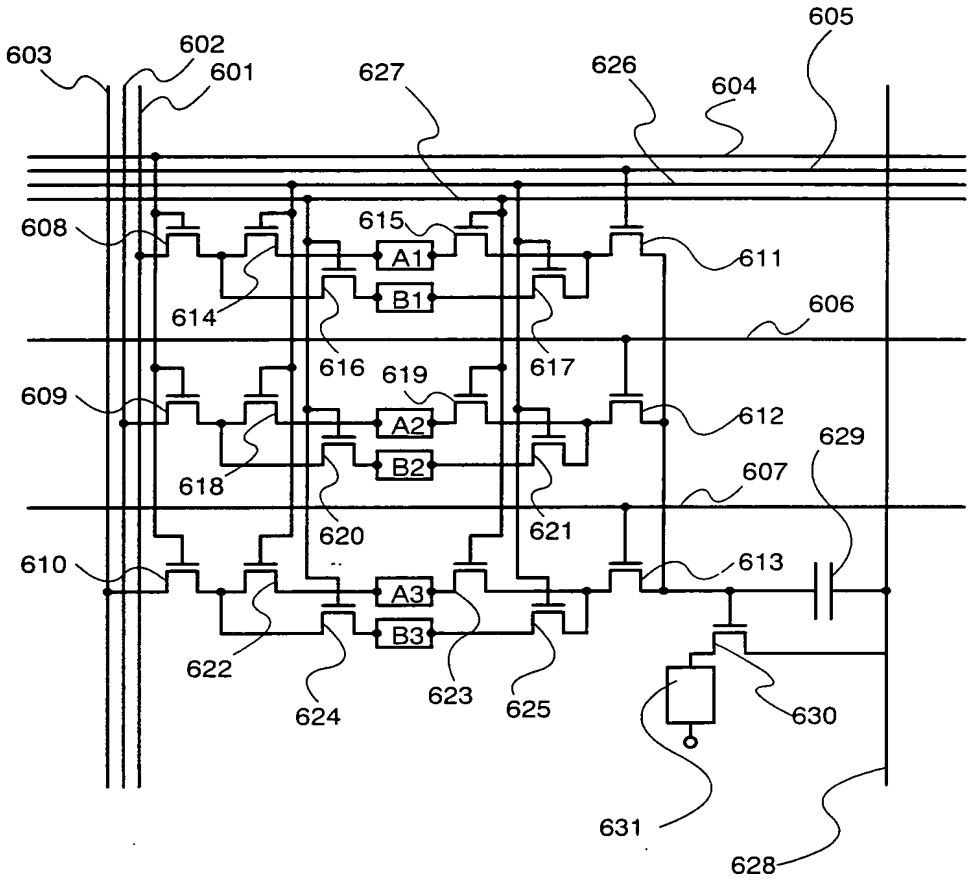

603
602
601
627
626
604
605
608
615
A1
611
B1
606
614
616
619
617
609
A2
612
629
618
B2
607
620
621
610
613
A3
B3
622
624
623
625
630
631
628

Fig. 7A

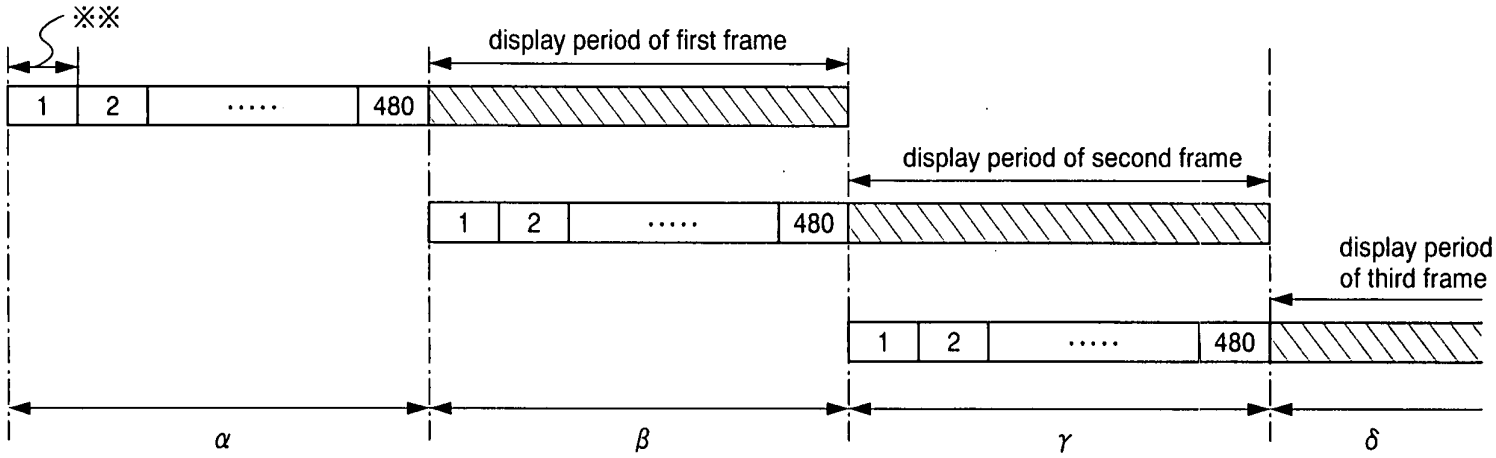


Fig. 7B

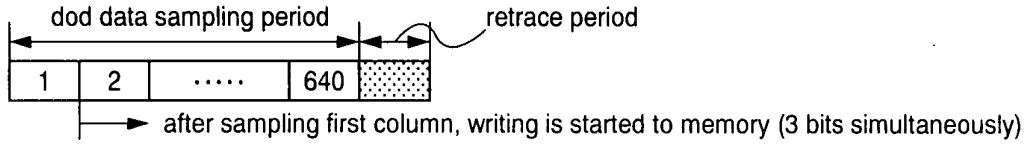


Fig. 7C

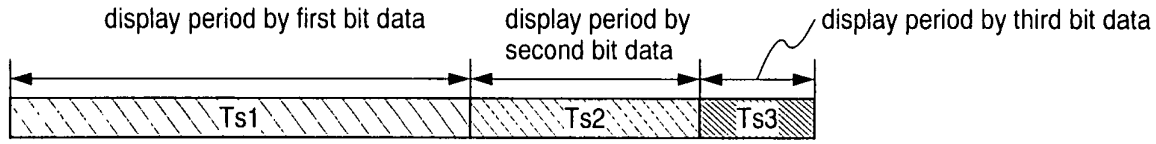


Fig. 8

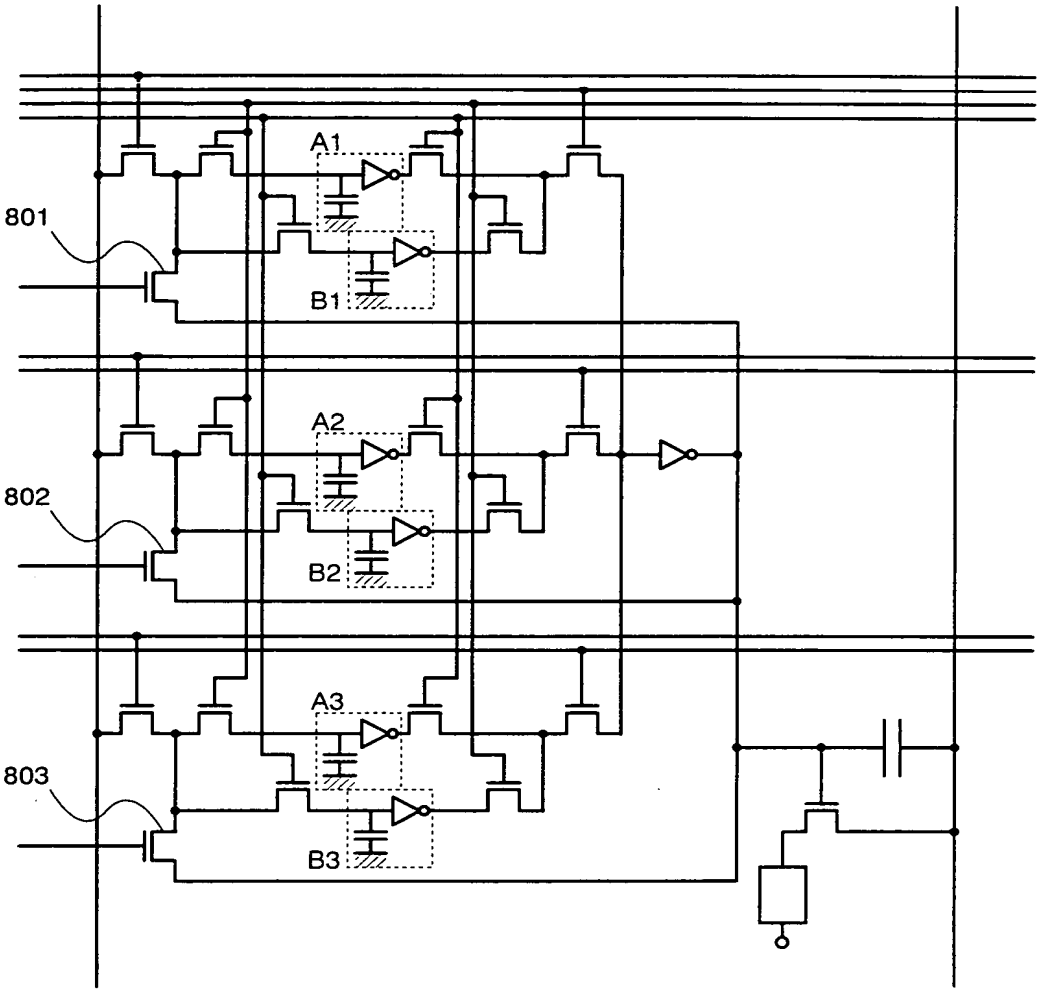


Fig. 9

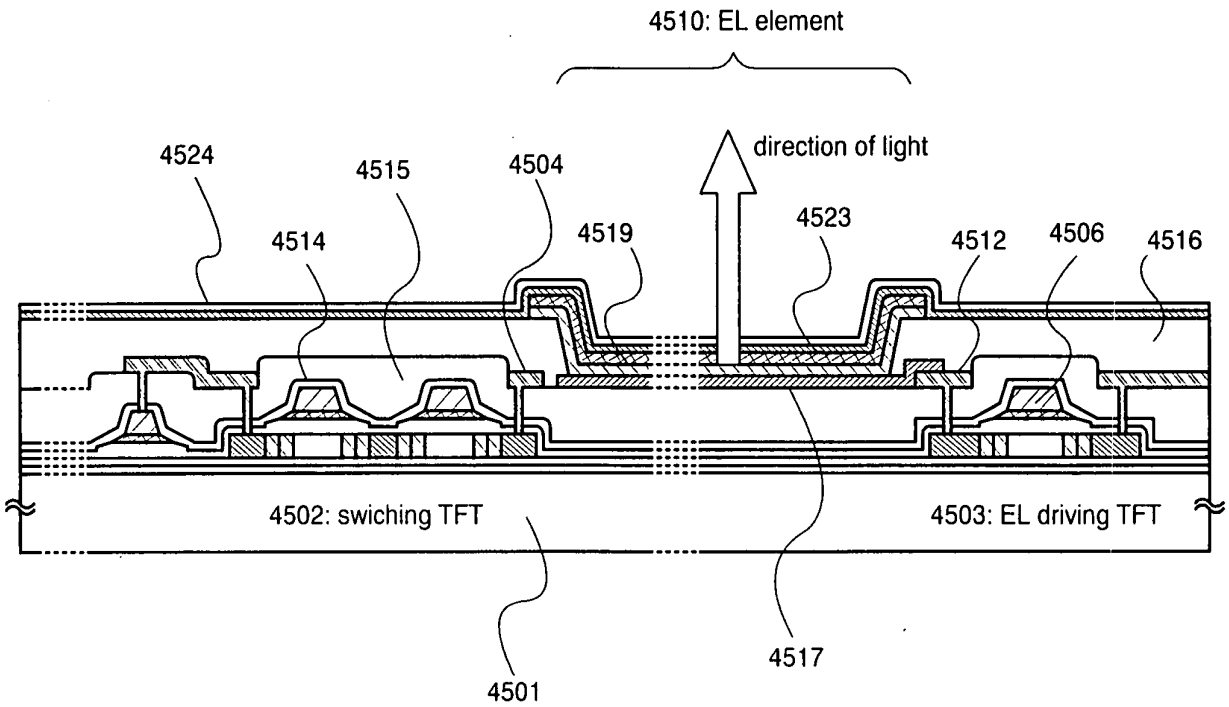

4510: EL element
direction of light
4524
4515
4504
4514
4519
4523
4512
4506
4516
4502: swiching TFT
4503: EL driving TFT
4501
4517

Fig. 10A

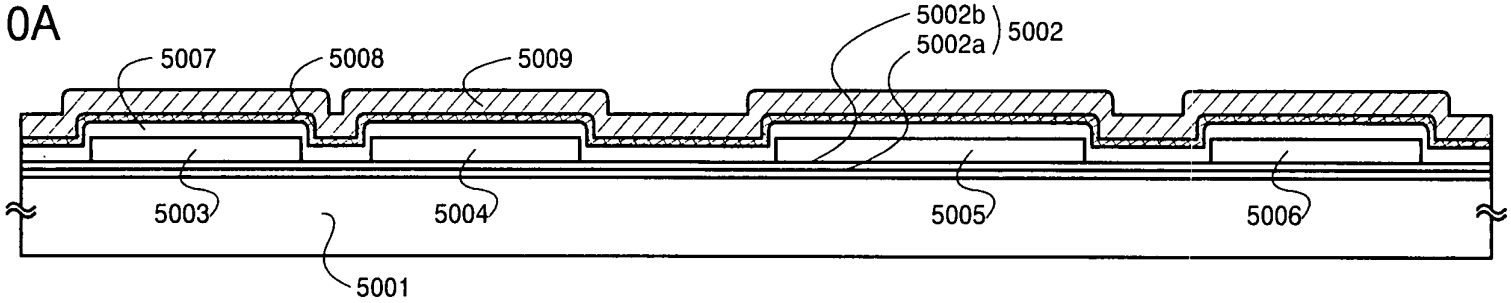


Fig. 10B

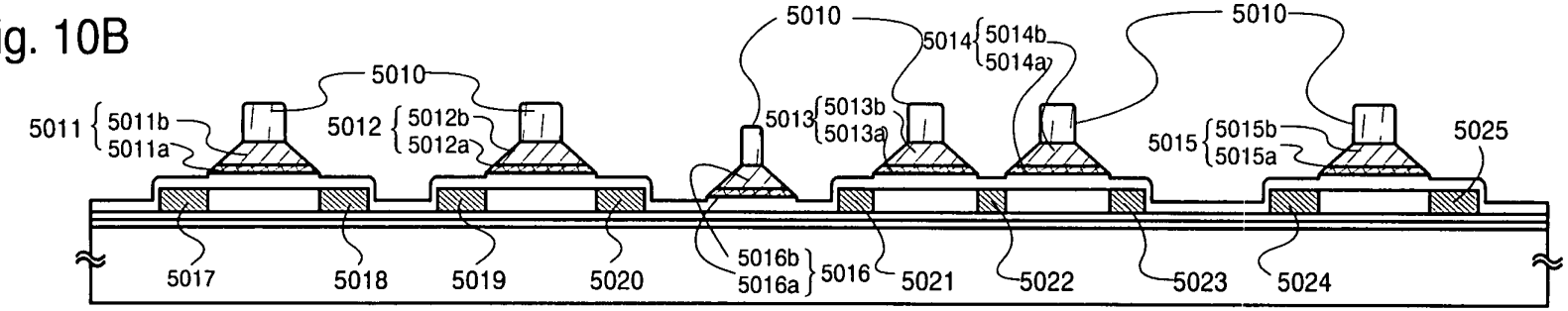


Fig. 10C

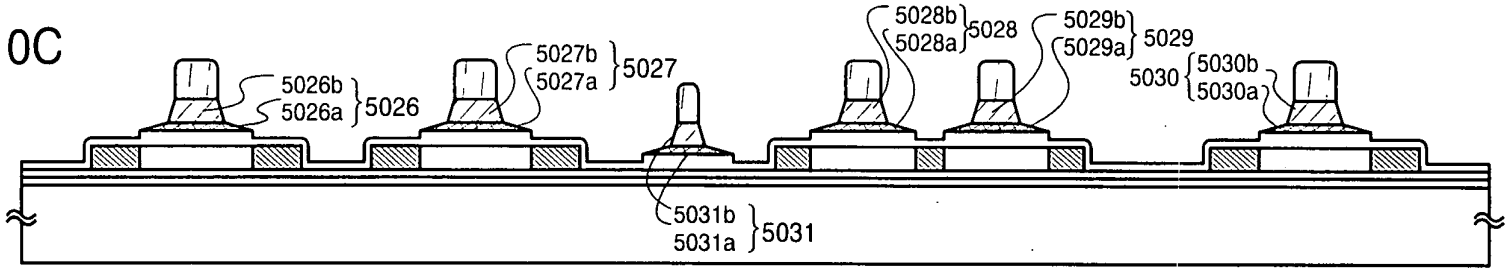


Fig. 11A

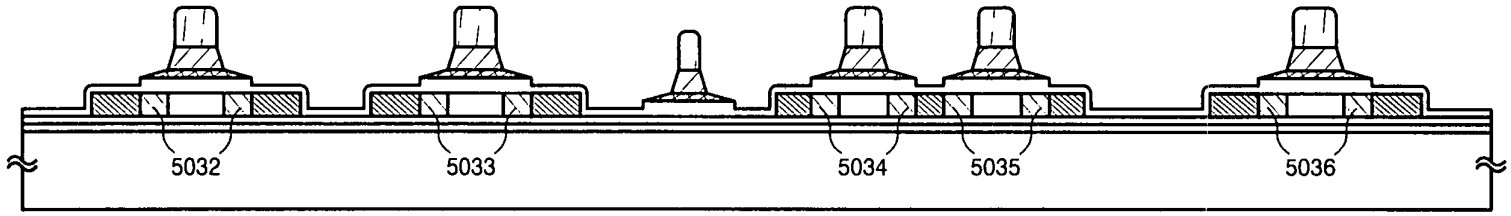


Fig. 11B

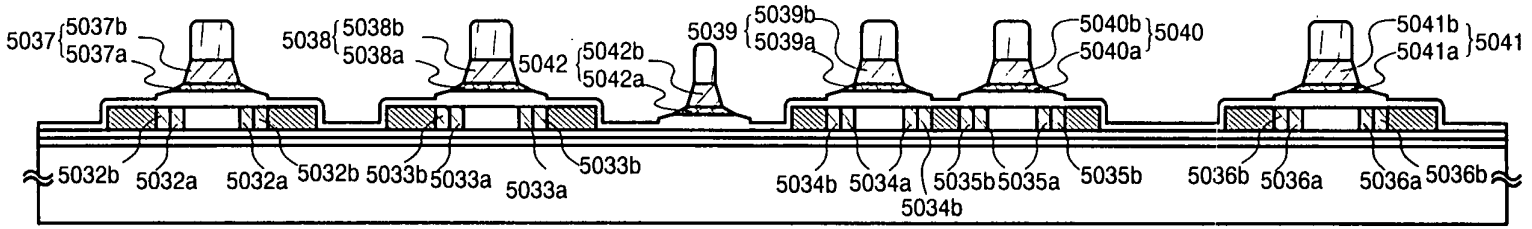


Fig. 11C

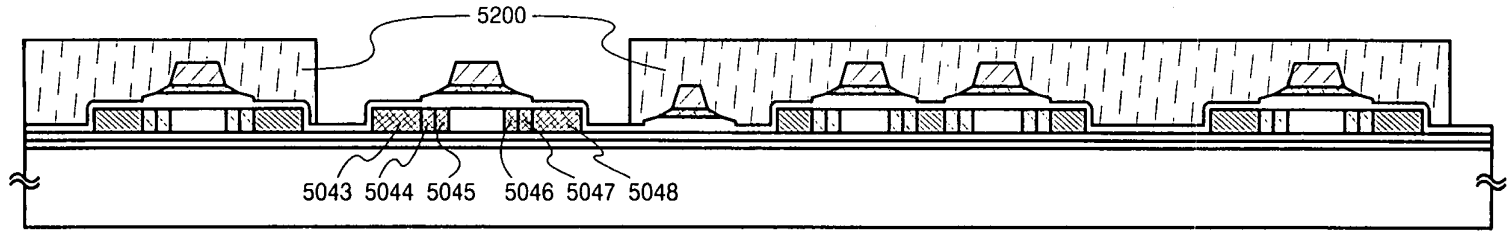


Fig. 12A

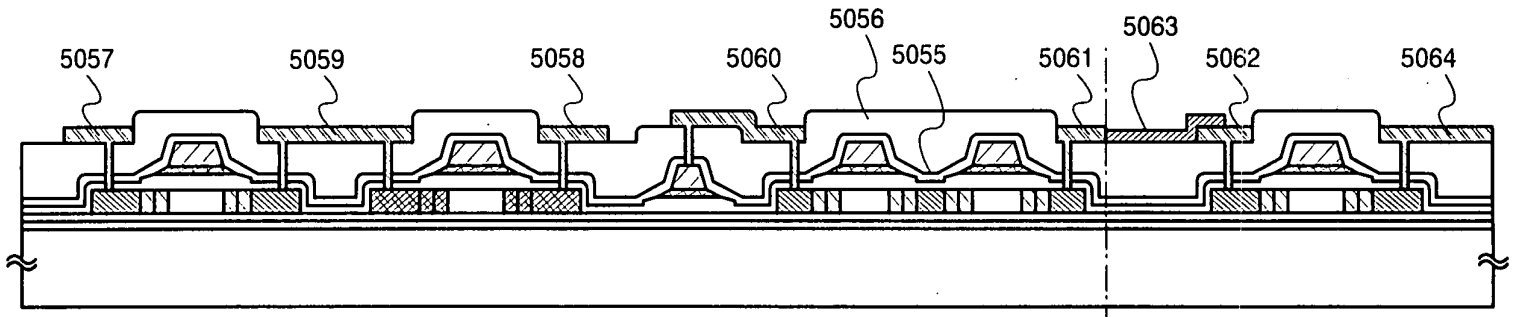


Fig. 12B

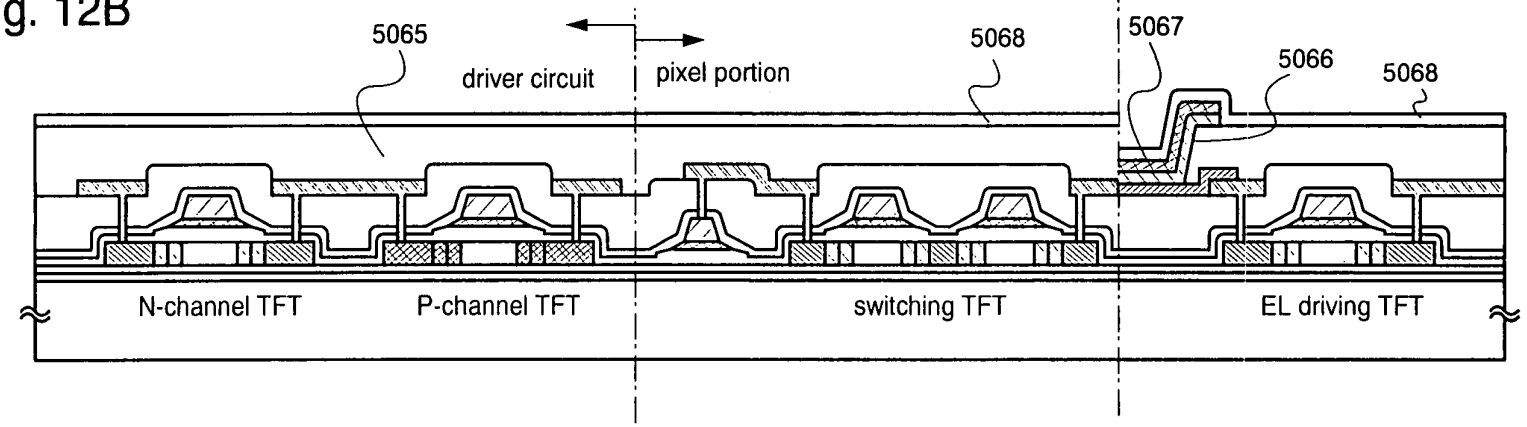


Fig. 13

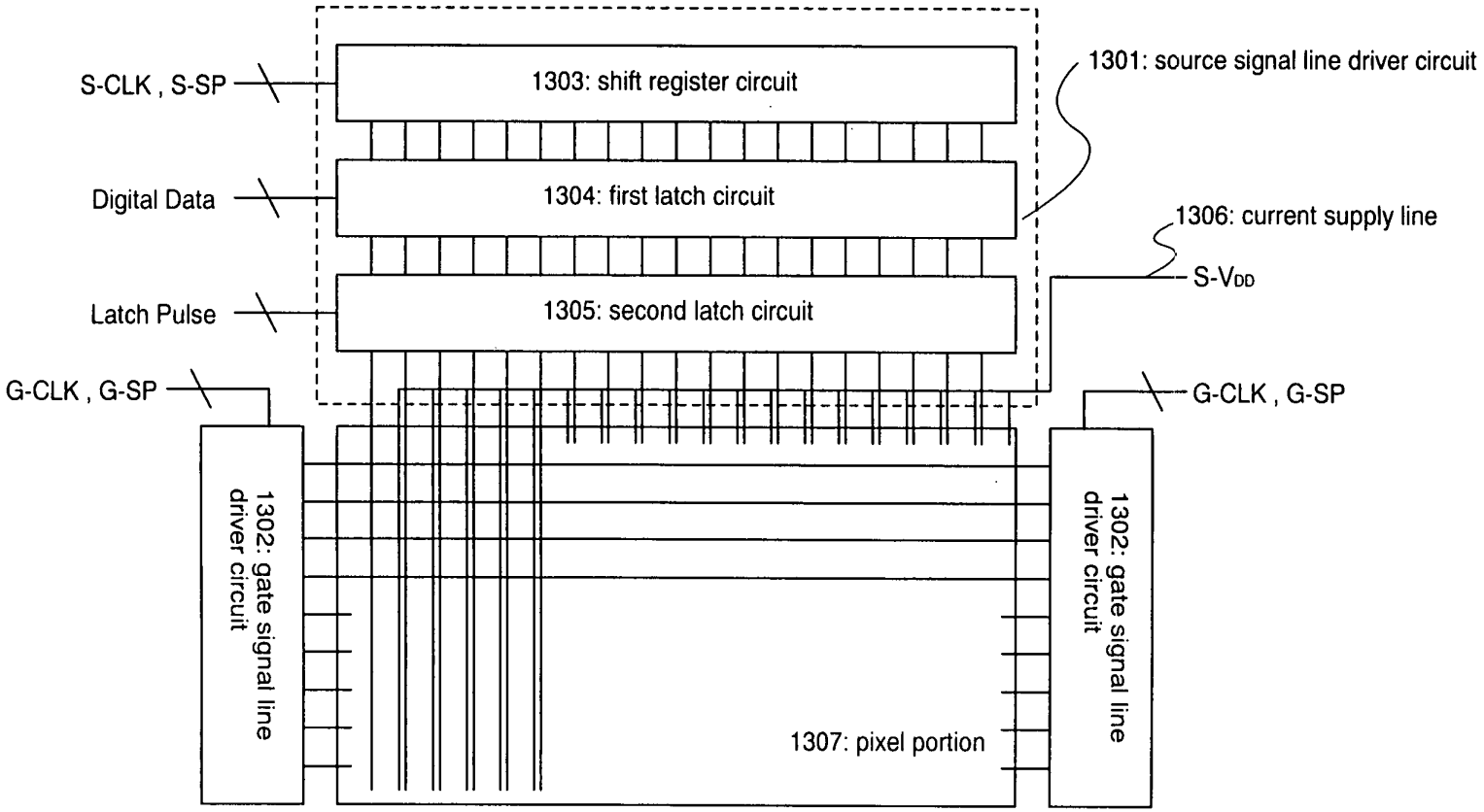
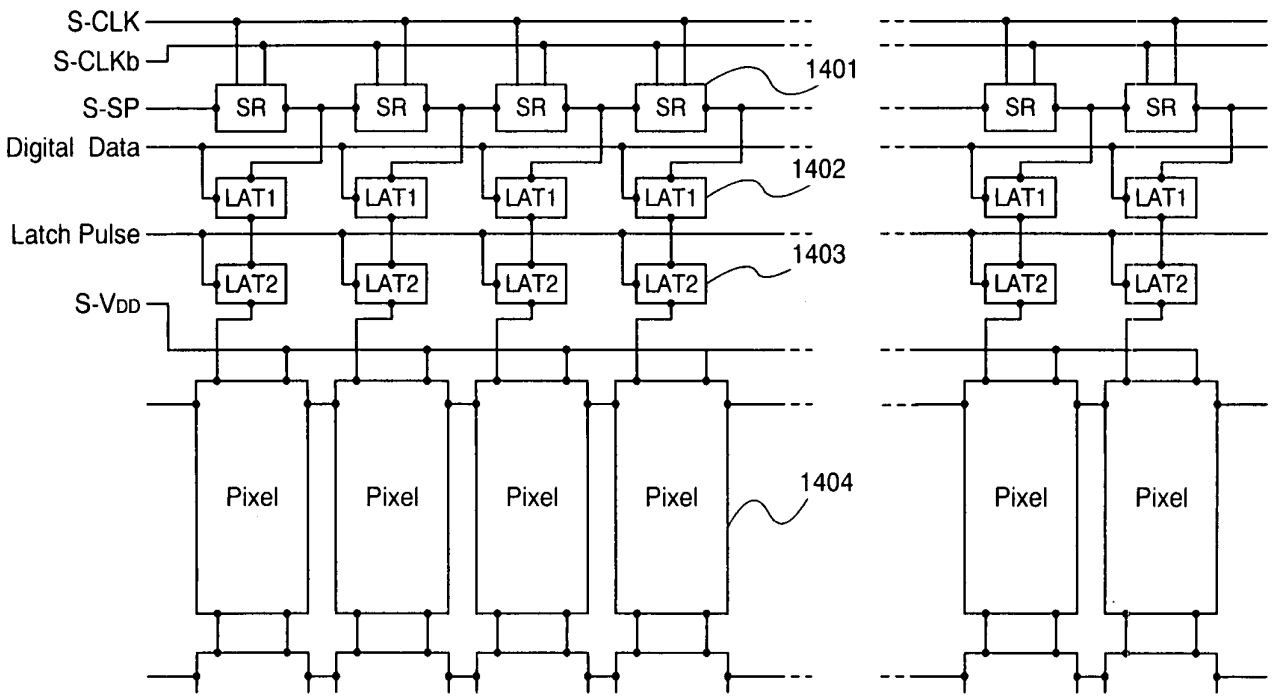

S-CLK , S-SP
Digital Data
Latch Pulse
G-CLK , G-SP
1303: shift register circuit
1304: first latch circuit
1305: second latch circuit
1301: source signal line driver circuit
1306: current supply line
S-VDD
G-CLK , G-SP
1302: gate signal line driver circuit
1302: gate signal line driver circuit
1307: pixel portion

Fig. 14


S-CLK
S-CLKb
S-SP
Digital Data
Latch Pulse
S-VDD
SR
LAT1
LAT2
Pixel
1401
1402
1403
1404

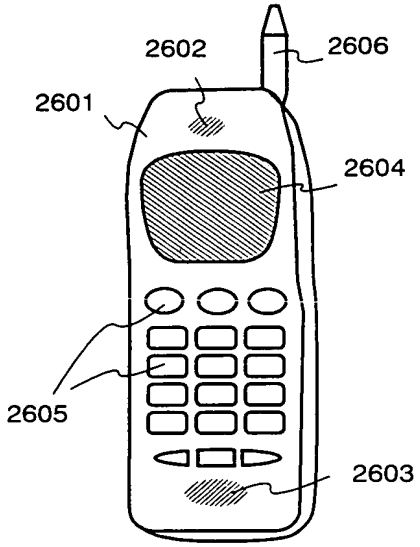


Fig. 15A

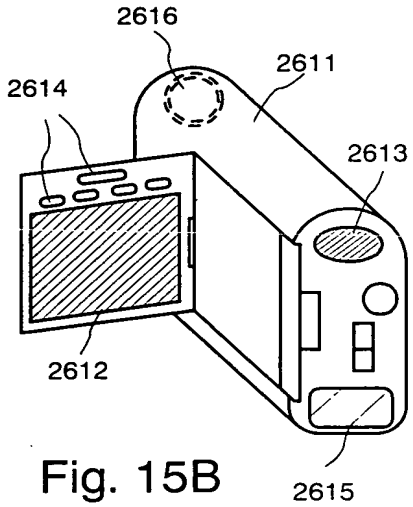


Fig. 15B

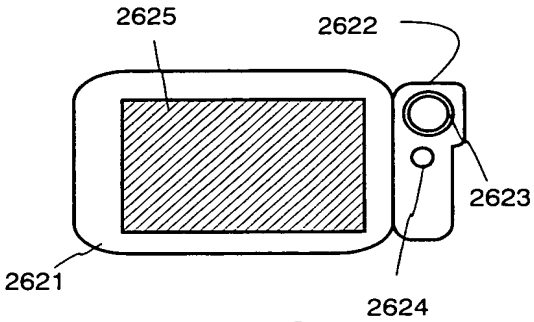


Fig. 15C

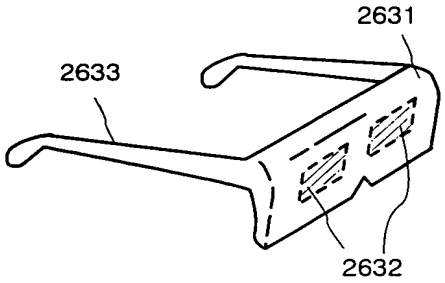


Fig. 15D

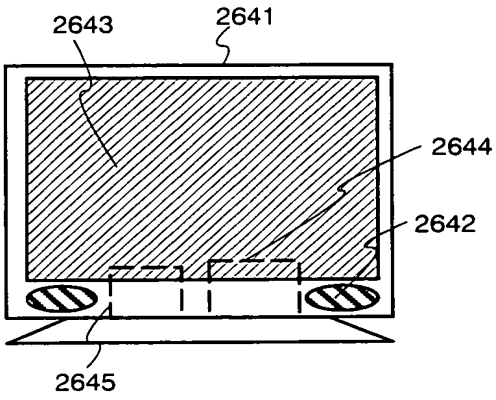


Fig. 15E

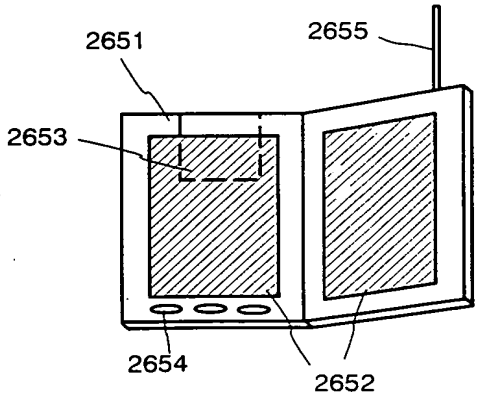


Fig. 15F

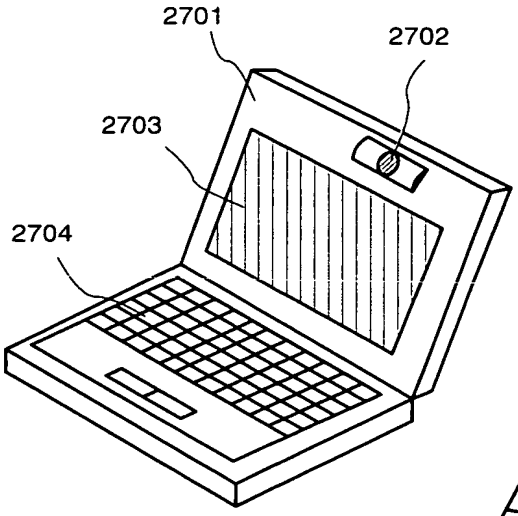


Fig. 16A

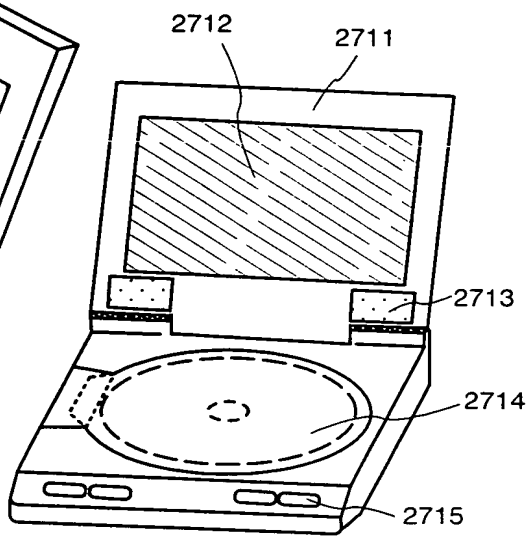


Fig. 16B

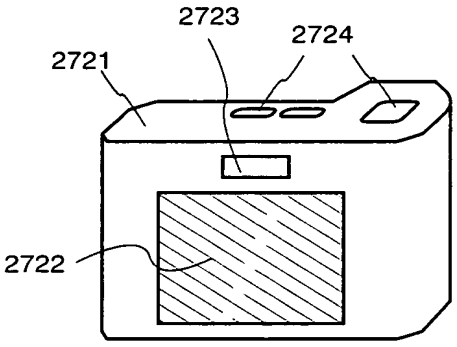


Fig. 16C

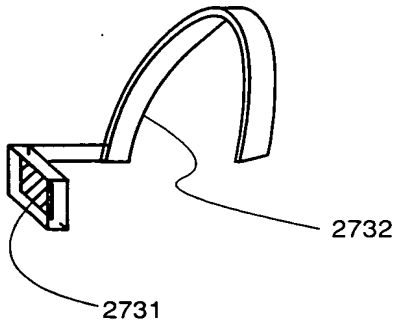


Fig. 16D

Fig. 17

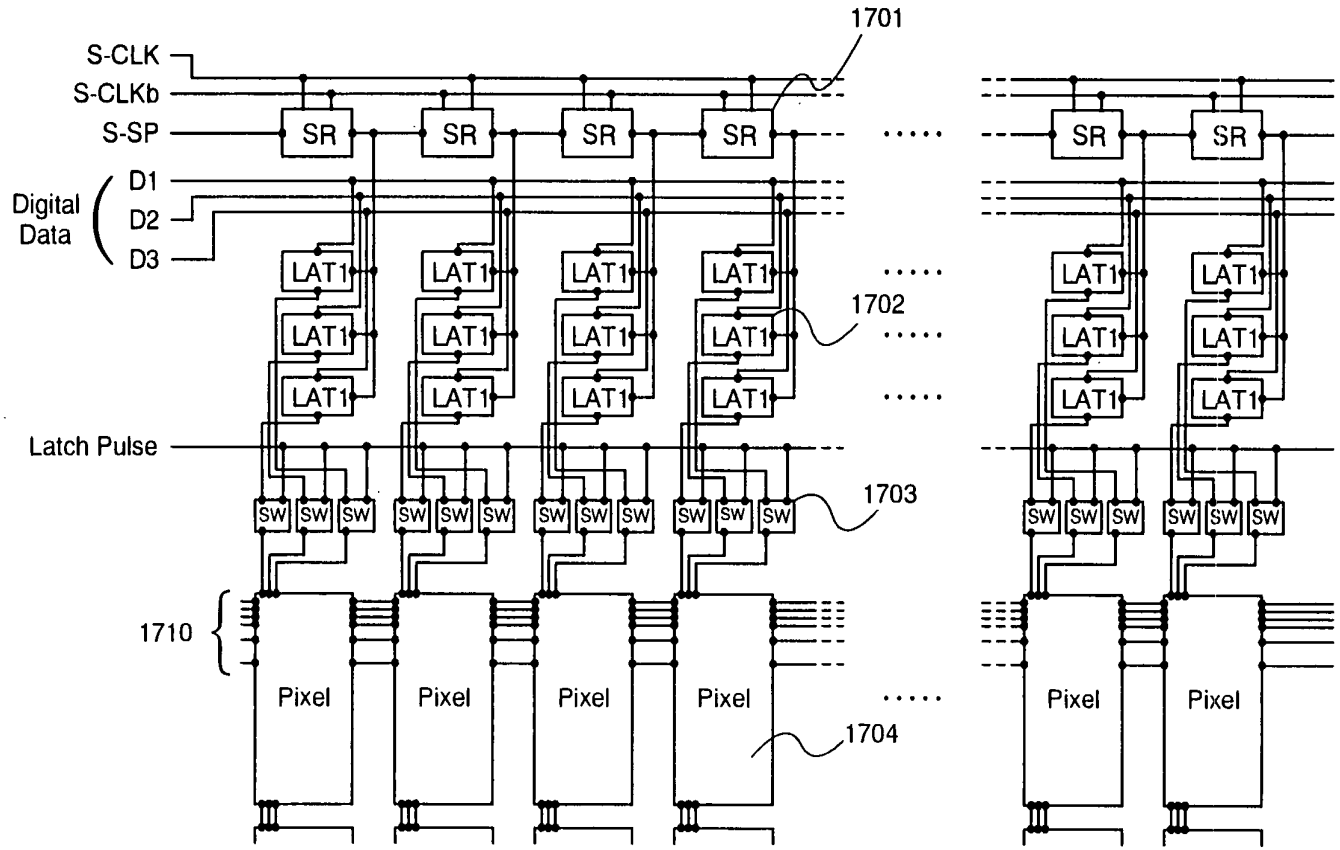

1701
S-CLK
S-CLKb
S-SP
Digital Data
D1
D2
D3
SR
LAT1
1702
Latch Pulse
SW
1703
1710
Pixel
1704

Fig. 18A

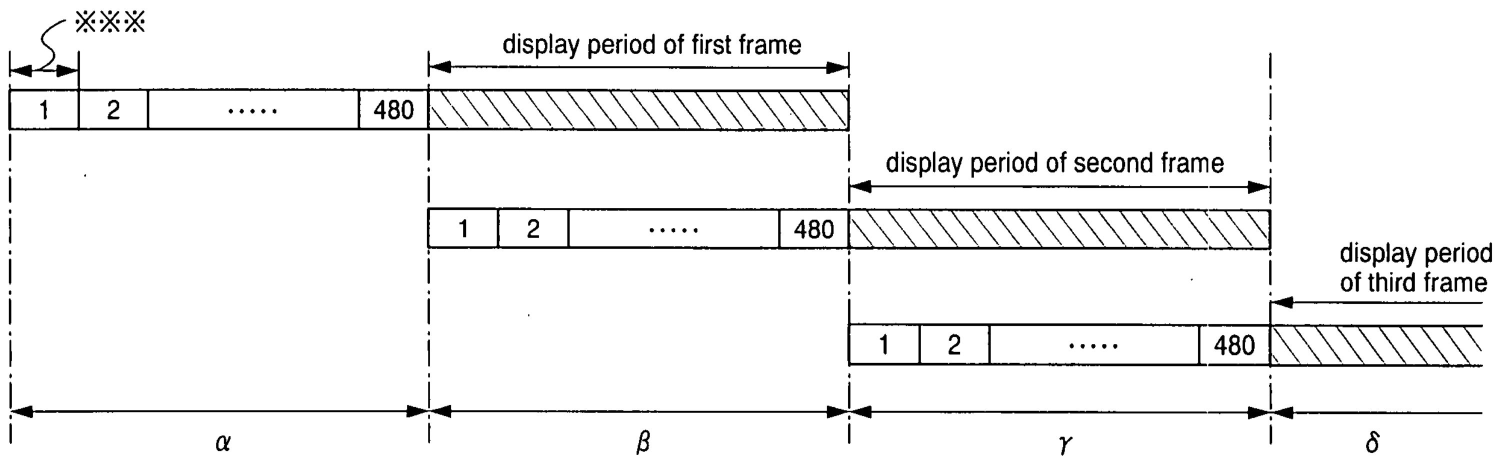


Fig. 18B

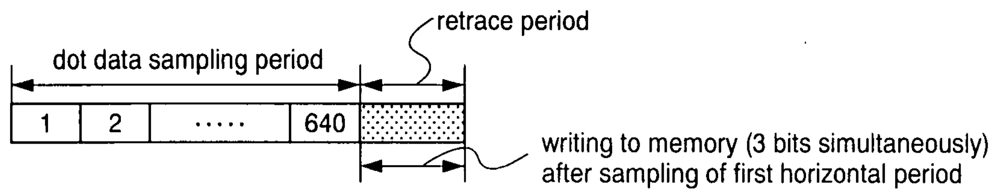


Fig. 18C

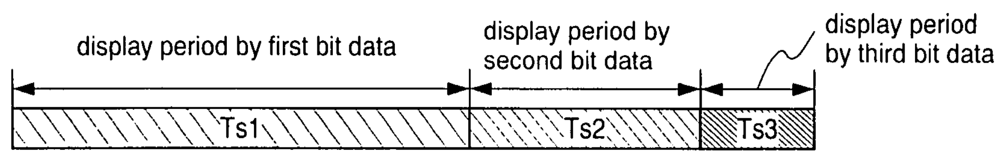


Fig. 19A

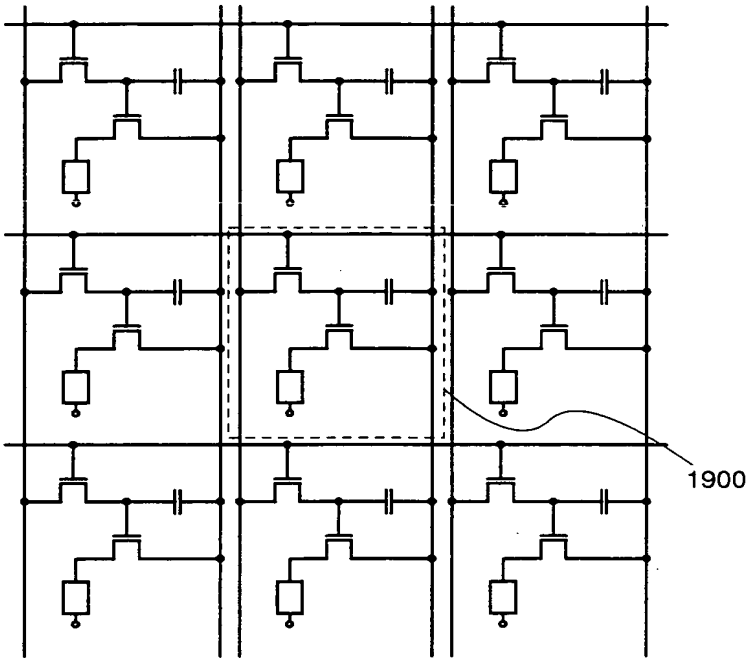


Fig. 19B

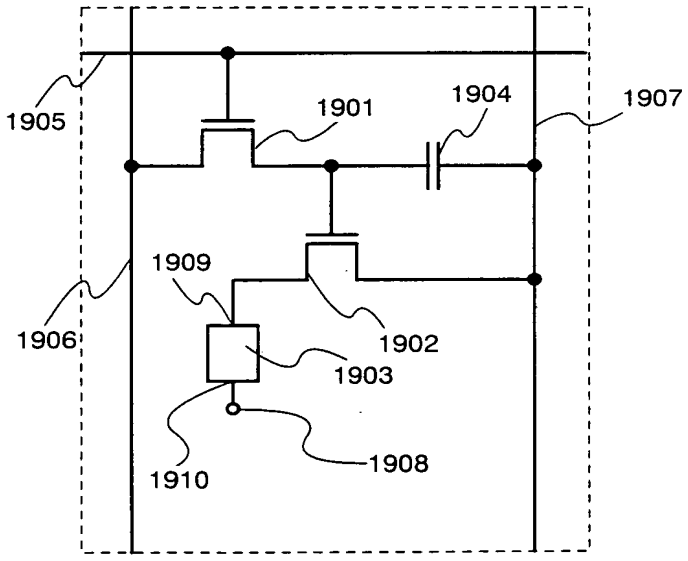


Fig. 20A

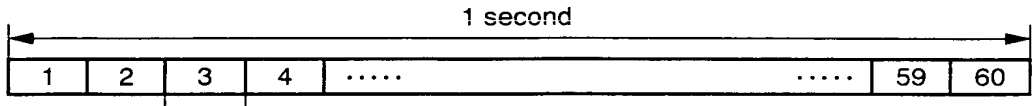


Fig. 20B

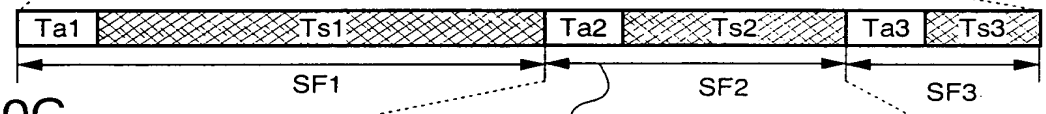


Fig. 20C

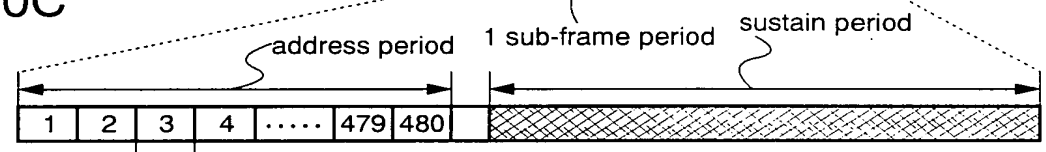


Fig. 20D

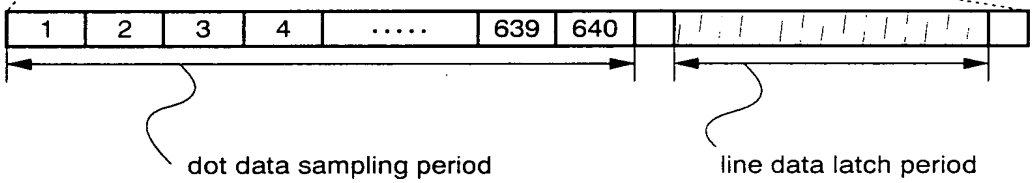
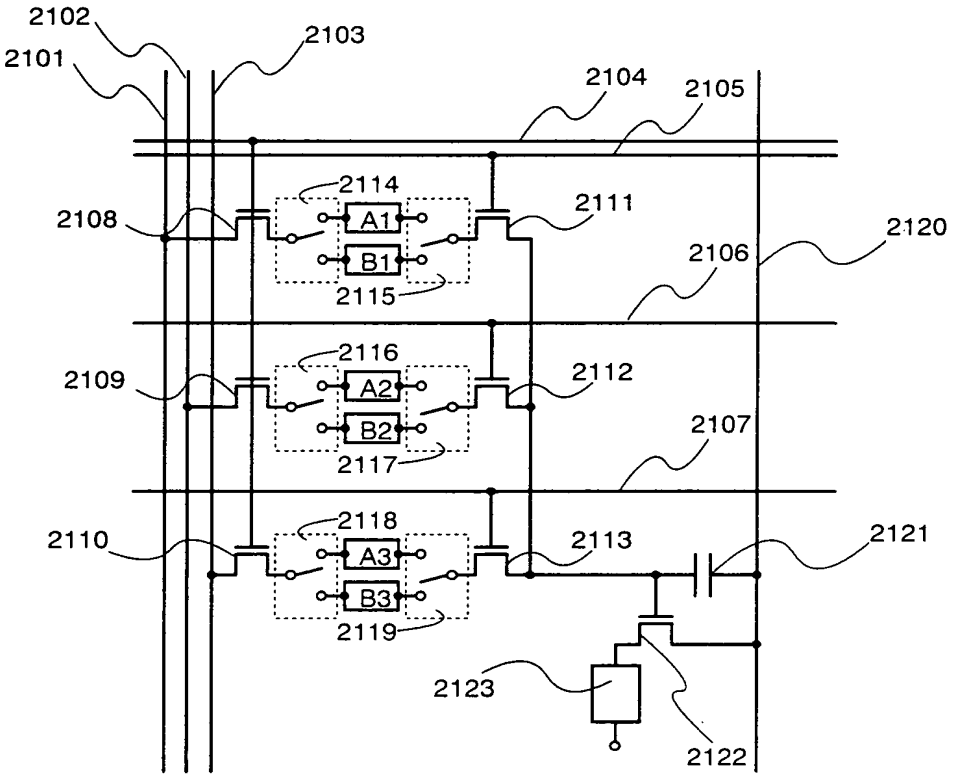


Fig. 21


2102
2103
2101
2104
2105
2114
2111
2108
A1
B1
2120
2106
2115
2116
2109
2112
A2
B2
2107
2117
2118
2110
2113
2121
A3
B3
2119
2123
2122